**INTRODUCTION TO XILINX ISE AND S3BOARD**

# LAB # 01



# Spring 2021

[**CSE-308L Digital System Design Lab**](https://classroom.google.com/u/0/c/MzA5OTAyNzE2MzM2)

Submitted by: **Hurair Mohammad**

Registration No. : **18PWCSE1657** Class Section: **B**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

# Engr. Madiha Sher

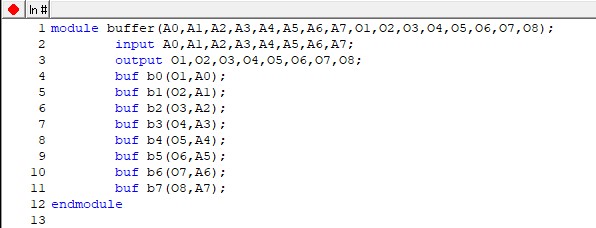
Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

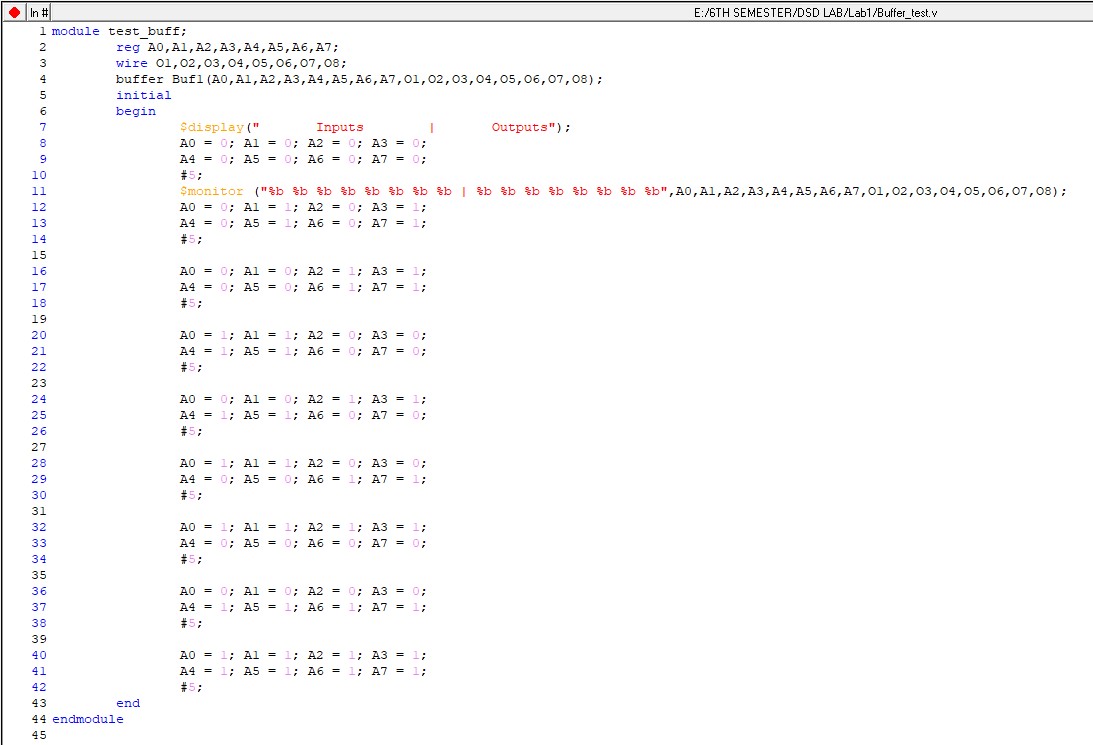
**OBJECTIVES:**

Introduction to FPGA and Xilinx

**CODE:**

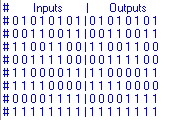


**TestBench:**

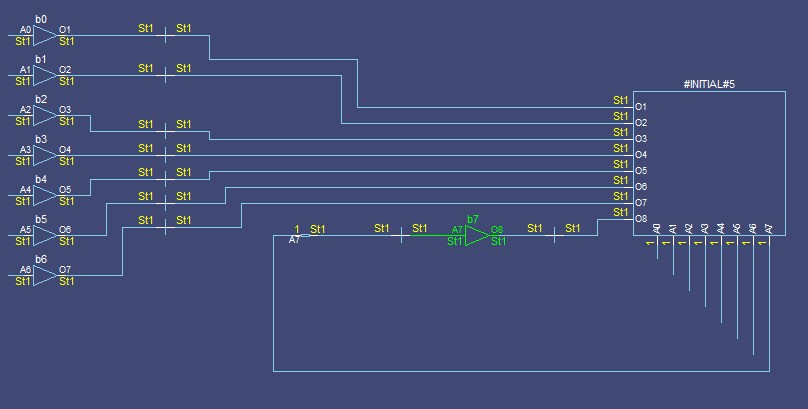


**OUTPUTS**

**Truth Table:**

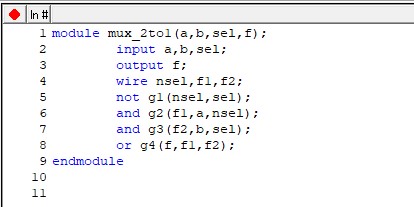


**Circuit Design:**

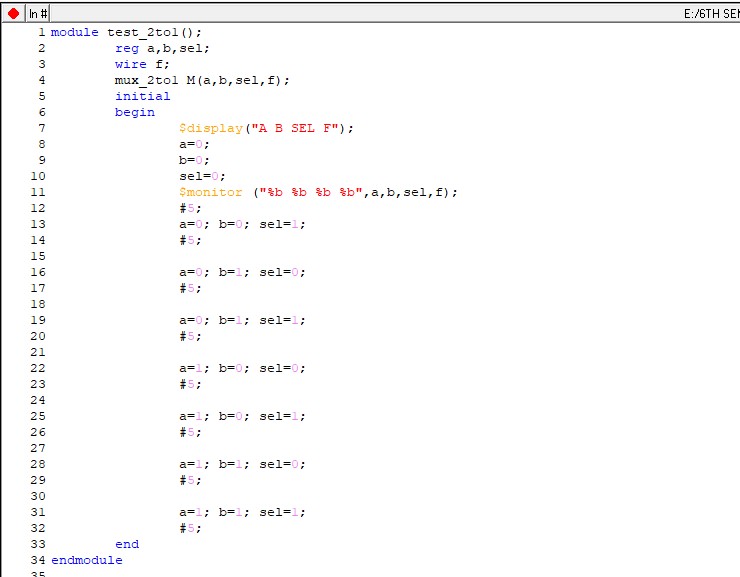


**TASK02:**

**CODE:**

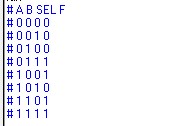


**TestBench:**

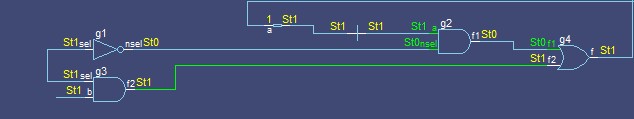


**OUTPUTS**

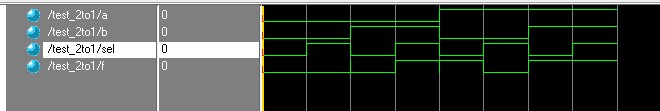
**Truth Table:**



**Circuit Design:**

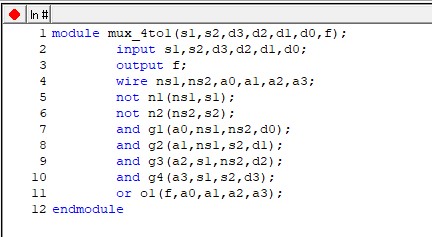


**Wave:**



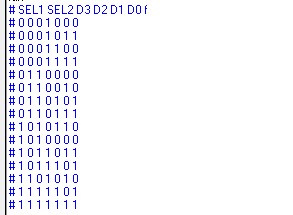
1. Implement 4x1 mux using modelsim.
   1. Simulate the multiplexer with a test bench.

**CODE:**

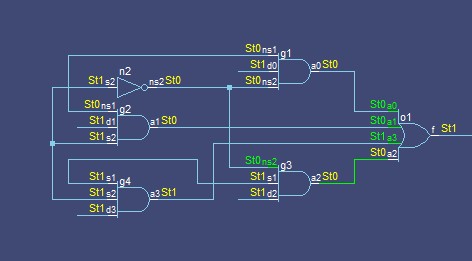


# OUTPUTS

**Truth Table:**



**Circuit Design:**



**Wave:**

